IN THE CLAIMS

1. (Withdrawn) A layout method of a semiconductor device comprising the steps of:

arranging active regions of a plurality of transistors, the active regions having at least more than one first and second electrodes disposed on a substrate;

arranging a plurality of gates of transistors between the more than one first and second electrodes of those active regions by positioning at least two or more gates having predetermined width and length at a substantially constant gap on the substrate; and

arranging a plurality of dummy gates having predetermined width and length between a plurality of transistors at substantially the same gap as that of the gates of transistors on the substrate.

2. (Withdrawn) The method, as defined in claim 1, wherein the length of the dummy gates is the same as that of the gates of the transistors.

3. (Withdrawn) The method, as defined in claim 1, wherein at least more than one gate of the plurality of transistors have common terminals each of which is commonly connected on the substrate of the semiconductor device.

4. (Withdrawn) The method, as defined in claim 1, wherein a plurality of dummy gates are commonly connected on the substrate.

5. (Withdrawn) A layout method of sense amplifier of a semiconductor device, wherein the sense amplifier amplifies and outputs the difference between the first and second input data applied by data input transistors and more than one control signal input transistors to which the control signals are applied, the method comprising the steps of:

arranging active regions of a plurality of transistors, the active regions having at least more than one first and second electrodes disposed on a substrate;

arranging a plurality of gates of transistors between more than one first and second electrodes of those active regions respectively by positioning two or more gates having predetermined width and length at a substantially constant gap on the substrate; and

arranging a plurality of dummy gates having predetermined width and length between the data and control signal input transistors at substantially the same gap as that of the gates divided from the data and control signal input transistors on the substrate.

6. (Withdrawn) The method, as defined in claim 5, wherein the dummy gates have a predetermined width, that is, the same as that of the gates which are largest in width among those divided gates of a plurality of transistors.

7. (Withdrawn) The method, as defined in claim 5, wherein the length of the dummy gates is substantially the same as that of the gates.

8. (Withdrawn) The method, as defined in claim 5, wherein at least more than one gate of the data and control signal input transistors have common terminals each of which is commonly connected on the substrate.

9. (Withdrawn) The method, as defined in claim 5, wherein a plurality of dummy gates are commonly connected on the substrate.

10. (Withdrawn) A layout method of a semiconductor device comprising the steps of:

arranging active regions of a plurality of transistors having at least more than one first and second electrodes disposed on a substrate;

arranging a plurality of gates of transistors between more than one first and second electrodes of those active regions respectively by positioning at least more than one gates having predetermined width and length at a substantially constant gap on the substrate; and

arranging a plurality of dummy gates having predetermined width and length between and outside a plurality of transistors at substantially the same gap as that of the gates of transistors on the substrate.

11. (Withdrawn) The method, as defined in claim 10, wherein the length of the gates of the transistors is substantially the same as that of the dummy gates.

12. (Withdrawn) The method, as defined in claim 10, wherein at least more than one gate of a plurality of transistors respectively have common terminals each of which is commonly connected on the substrate of the semiconductor device.

13. (Withdrawn) The method, as defined in claim 10, wherein a plurality of dummy gates are commonly connected on the substrate.

14. (Previously presented) A semiconductor device comprising:

a substrate;

a plurality of active regions each having ~~of~~ at least two transistors~~,~~ and at least two electrodes disposed on the substrate;

a plurality of transistor gates disposed on the substrate in each active region between the at least two electrodes, wherein at least two transistor gates are of a predetermined width and length and separated by a substantially identical gap with no intervening structures between the at least two transistor gates; and

a plurality of dummy gates having the predetermined width and length and located between the at least two transistors, wherein at least two dummy gates are separated from an adjacent transistor gate by the ~~at a~~ substantially identical gap, and wherein the plurality of dummy gates are separated from each other by the substantially identical gap.

15. (Previously presented) The device, as defined in claim 14, wherein the length of the dummy gates is substantially the same as that of the transistor gates.

16. (Previously presented) The device, as defined in claim 14, wherein at least two gate transistors of each of the at least two transistors has a common terminals, the common terminal commonly connected on the substrate.

17. (Previously presented) The device, as defined in claim 14, wherein the plurality of dummy gates is commonly connected on the substrate.

18. (Previously presented) A semiconductor device comprising:

a substrate;

a plurality of active regions ~~of~~ comprising at least two transistors, the active regions having at least two electrodes disposed on the substrate;

a plurality of transistor gates disposed between the at least two electrodes, the transistor gates being positioned such that at least two transistor gates ~~is~~ are of a predetermined width and length ~~at~~ with a substantially identical gap separating the at least two transistor gates with no intervening structures between the at least two transistor gates; and

a plurality of dummy gates having the predetermined width and length and located between and to either side of the at least two transistors, wherein at least four dummy gates are separated from an adjacent transistor gate by the substantially identical gap, and wherein each of the plurality of dummy gates is separated from another dummy gate by the substantially identical gap.

19. (Previously presented) The device, as defined in claim 18, wherein the length of the dummy gates is substantially the same as that of the transistor gates.

20. (Previously presented) The device, as defined in claim 18, wherein at least two gate transistors of each of the at least two transistors has a common terminal the common terminal commonly connected on the substrate.

21. (Previously presented) The device, as defined in claim 18, wherein the plurality of dummy gates is commonly connected on the substrate.

22. (Previously presented) A semiconductor device comprising:

a substrate;

a plurality of active regions ~~of~~ comprising at least two transistors having at least more than one first and second two electrodes disposed on the substrate;

a plurality of transistor gates disposed between the at least two electrodes, the transistor gates being positioned such that at least two transistor gates ~~has~~ have a predetermined width and length ~~at~~ with a substantially identical gap separating the at least two transistor gates with no intervening structures between the at least two transistor gates; and

a plurality of dummy gates having the predetermined width and length and located not between but to both sides of the at least two transistors, wherein at least two dummy gates are separated from an adjacent transistor gate by the ~~at a~~ substantially identical gap, and wherein each of the plurality of dummy gates is separated from another dummy gate by the substantially identical gap.

23. (Original) The device, as defined in claim 22, wherein the length of the dummy gates is substantially the same as that of the transistor gates.

24. (Original) The device, as defined in claim 22, wherein at least more than one gate of a plurality of transistors respectively have common terminals each of which is commonly connected on the substrate.

25. (Original) The device, as defined in claim 22, wherein a plurality of dummy gates are commonly connected on the substrate.

Claims 26-28. (Cancelled)

29. (Currently Amended) A semiconductor device comprising:

a substrate with a plurality of active regions and a plurality of inactive regions, each active region having at least one source region and at least one drain region;

a plurality of transistor gates, each transistor gate having at least one ~~or more~~ gate ~~extensions~~ extension that extends over one of the plurality of active regions between the at least one source region and the at least one drain region; and

a plurality of dummy gates, each dummy gate having at least one ~~or more~~ dummy gate ~~extensions~~ extension that extends over one of the plurality of inactive regions, ~~wherein~~ where each of the ~~one or more~~ dummy gate extensions and each of the ~~one or more~~ gate extensions ~~are substantially parallel, and wherein each of the gate extensions and dummy gate extensions have substantially identical spacing across the substrate~~ are elements of a group, where each element of the group is parallel to at least two other elements of the group and all elements of the group are uniformly spaced across a width of the substrate.

30. (Previously presented) The device, according to claim 29, in which a first metal is connected to the at least one source region and the at least one drain region by a plurality of contacts.

31. (Previously presented) The device, according to claim 30, in which a second metal is connected to a first part of the first metal to supply a voltage.

32. (Previously presented) The device, according to claim 31, in which the plurality of dummy gates are commonly connected by a second part of the first metal to supply a ground voltage.

33. (Previously presented) A semiconductor device comprising

a substrate;

a first region having a plurality of first active regions each having a source region and a drain region respectively and a first portion other than the plurality of first active regions on the substrate;

a second region having a plurality of second active regions each having a source region and a drain region respectively and a second portion other than the plurality of second active regions on the substrate;

a plurality of first transistor gates formed on the plurality of first active regions, disposed between the source region and the drain region, the plurality of first transistor gates being characterized by a first gap between neighboring first transistor gates and without intervening structure between neighboring first transistor gates;

a plurality of second transistor gates formed on the plurality of second active regions, the plurality of second transistor gates also being characterized by the first gap between neighboring second transistor gates;

a plurality of first dummy gates formed on the first portion, the plurality of first dummy gates being characterized by a second gap between neighboring first dummy gates and without intervening first transistor gates between neighboring first dummy gates;

a plurality of second dummy gates formed on the second portion, the plurality of second dummy gates also being characterized by the second gap between neighboring second dummy gates without intervening second transistor gates between neighboring second dummy gates;

wherein a first transistor gate at an edge of the first active regions is separated from a first dummy gate at an edge of the first portion by a third gap, wherein a second transistor gate at an edge of the second active region is separated from a second dummy gate at an edge of the second portion by a fourth gap, and wherein the first, second, third, and fourth gaps are substantially identical;

a first metal connected to the source and drain regions by a contact; and

a second metal connected to a first part of the first metal to supply a voltage.

34. (Previously presented) The semiconductor device according to claim 33, in which the first gap is substantially identical to the second gap.

35. (Previously presented) The semiconductor device according to claim 33, in which the second metal is connected to a second part of the first metal to supply a ground voltage.

36. (Currently Amended) A semiconductor device comprising:

a substrate having a plurality of active regions;

a plurality of ~~divided~~ gates ~~for a plurality of transistors~~ disposed on the active regions, each gate having at least one gate extension; and;

a plurality of dummy ~~divided~~ gates disposed on the substrate, each dummy gate having at least one dummy gate extension, wherein each of the ~~plurality of~~ dummy ~~divided gates substantially fills a region on the substrate devoid of divided gates, and wherein~~ gate extensions and each of the ~~divided gates and dummy divided gates are substantially complementary such that they form a uniform pattern over the substrate~~ gate extensions are

elements of a group, each element of the group being located on one of a plurality of parallel lines and all elements of the group spaced uniformly across a width of the substrate.

37. (Currently Amended) The semiconductor device according to claim 36, wherein a length of the ~~divided gates~~ gate extensions and the dummy ~~divided gates~~ gate extensions is variable.

38. (Currently Amended) The semiconductor device according to claim 37, wherein a width of the ~~divided gates~~ gate extensions and the dummy ~~divided gates~~ gate extensions is substantially the same.

39. (Cancelled)

40. (Previously presented) A semiconductor device comprising:

a substrate;

a plurality of active regions having at least two transistors and two electrodes disposed on the substrate;

a plurality of transistor gates of a first width disposed on the substrate between the at least two electrodes of the active regions

a plurality of dummy gates of a second width disposed on the substrate between the at least two electrodes of the active regions; and

a plurality of dummy gates of a third width disposed on the substrate between the at least two electrodes of the active regions, wherein each of the transistor gates is aligned along the same longitudinal axis as a corresponding one of the dummy gates of a third width, and wherein the second width is greater than the sum of the first and third widths.

41. (Previously presented) The semiconductor device according to claim 40, in which the plurality of transistor gates and of the plurality dummy gates are of substantially identical gap between gates.

42. (Previously presented) The device, as defined in claim 40, wherein the length of the dummy gates is substantially the same as that of the transistor gates.

43. (Previously presented) The device, as defined in claim 40, wherein at least more than one gate of a plurality of transistors respectively have common terminals each of which is commonly connected on the substrate.

44. (Previously presented) The device, as defined in claim 40, wherein a plurality of dummy gates are commonly connected on the substrate.

45. (Previously presented) The device, as defined in claim 40, wherein the width of the dummy gates is substantially the same as that of the transistor gates.

46. (Currently Amended) A semiconductor device comprising:

a substrate;

~~a plurality of active regions having at least two transistors and at least two electrodes disposed on the substrate;~~

a plurality of transistor gates disposed on the substrate ~~between the at least two electrodes of the active regions, wherein at least two transistor gates have~~ each transistor gate having at least one gate extension that has an elongated length relative to width; and

a plurality of dummy gates disposed on the substrate, each dummy gate ~~having a first portion~~ in contact with a bias line~~,~~ and ~~each dummy gate~~ having at least one ~~second portion extending parallel to the elongated length of the at least two transistor gates, wherein a first adjacent transistor gate on one side of a dummy gate and a second adjacent transistor gate on another side of the dummy gate are equidistant from the dummy gate~~ dummy gate extension, each of the gate extensions and each of the dummy gate extensions being an element of a group, where all elements of the group are oriented in the same direction and all elements of the group are uniformly spaced across a width of the substrate.

47. (Cancelled)

48. (Currently Amended) The device, as defined in claim 46, wherein the length of the ~~dummy gates~~ dummy gate extensions is substantially the same as that of the ~~transistor gates~~ gate extensions.

49. (Currently Amended) The device, as defined in claim 46, wherein at least ~~more than one gate of a plurality of transistors respectively~~ two transistor gates have a common ~~terminals each of which is commonly connected on the substrate~~ terminal.

50. (Currently Amended) The device, as defined in claim 46, wherein ~~a~~ the plurality of dummy gates are commonly connected ~~on the substrate~~.

51. (Currently Amended) The device, as defined in claim 46, wherein ~~the~~ a width of the dummy ~~gates~~ gate extensions is substantially the same as that of the ~~transistor gates~~ gate extensions.

52. (Previously presented) A semiconductor device comprising:

a substrate;

a plurality of active regions having at least two transistors and at least two electrodes disposed on the substrate;

a plurality of transistor gates disposed on the substrate between the at least two electrodes of the active regions at least two transistor gates have a first portion extending in a first direction and a plurality of second portions extending in a second direction perpendicular to the first direction; and

a plurality of dummy gates disposed on the substrate between the at least two electrodes of the active regions, each dummy gate having a first portion extending in the first direction and a plurality of second portions extending in the second direction perpendicular to the first direction;

wherein a gap between adjacent second portions of the at least two transistor gates and a gap between adjacent second portions of the dummy gates are substantially identical to a gap between a second portion of a transistor gate and an adjacent second portion of a dummy gate

wherein a physical dimension of the second portions of the at least two transistor gates in the first direction is substantially identical to a physical dimension of the second portions of the plurality of dummy gates in the first direction;

and wherein the plurality of transistor gates and the plurality of dummy gates are commonly connected on the substrate, respectively.

53. (Previously presented) A semiconductor device comprising:

a substrate;

a plurality of active regions having at least two transistors and at least two electrodes disposed on the substrate;

a plurality of transistor gates disposed on the substrate between the at least two electrodes of the active regions, at least two transistor gates having a first portion extending in a first direction and a plurality of second portions extending in a second direction perpendicular to the first direction ; and

a plurality of dummy gates, each having a first portion extending in the first direction and in contact with a bias line, each having at least one second portions extending in the second direction and disposed on the substrate such that the at least one second portion is interspaced between the at least two transistors;

wherein a gap between adjacent second portions of the at least two transistor gates and a gap between adjacent second portions of the dummy gates are substantially identical to a gap between a second portion of a transistor gate and an adjacent second portion of a dummy gate

wherein a physical dimension of the second portions of the at least two transistor gates in the first direction is substantially identical to a physical dimension of the second portions of the plurality of dummy gates in the first direction;

and wherein the plurality of transistors and the plurality of dummy gates are commonly connected on the substrate, respectively.

54. (Previously presented) A semiconductor device comprising:

a substrate;

a rectangular region on the substrate;

an active region having a first width and a second width on said rectangular region;

an isolation portion of said active region on said rectangular region;

first transistor gates on said first width of said active region;

second transistor gates on said second width; and

first dummy gates on said isolation portion aligned with said first transistor gates such that a portion of a first dummy gate extending in a first direction and a portion of a corresponding first transistor gate extending in the first direction share a common central axis;

wherein said first width is less than said second width;

and wherein said transistor gates and said first dummy gates are of substantially identical gap between gates.

55. (Previously presented) The device of claim 54 wherein said active region is n-type.

56. (Previously presented) The device of claim 54 wherein said active region is p-type.

57. (Previously presented) The device of claim 54, further comprising:
second dummy gates on said rectangular region having a substantially identical width as said second transistor gates.

58. (Previously presented) The device of claim 57 wherein said active region is n-type.

59. (Previously presented) The device of claim 57 wherein said active region is p-type.